Details of the Programme: **Add-on Course in Semiconductor Technology**

1. Duration: 2 Year (Annual Mode)

16 Credits (1 Year) → Add-on Certificate Level Course in Semiconductor Technology

32 Credits (2 Years) → Add-on Diploma Level Course in Semiconductor Technology

2. Programme Objectives aims at:

Equip students with a solid foundation in semiconductor physics.

Provide in-depth knowledge of key semiconductor manufacturing processes such as photolithography, doping, etching, deposition, and packaging.

Introduce quality control, process monitoring, and testing techniques used in the semiconductor industry to ensure reliability and performance.

Prepare students for employment in the semiconductor and electronics industries through internships, industrial visits, and soft skills training.

Encourage analytical thinking and innovation in troubleshooting semiconductor process issues and improving device performance.

3. Eligibility: **Registered PG Students in University Teaching Department (Physical Sciences) with Physics as one of the subjects in the under graduation programme.**

4. Admission Process: Based on merit/entrance test/interview, as decided by the university/department.

5. Duration and Exit Options

After completion of one year, an option of exit with an Add-on certificate **level course** in Semiconductor Technology subject to completion of 16 credits course (Annual mode).

On successful completion of 2 years, an Add-on Diploma **level course in Semiconductor Technology** will be awarded.

6. Credit Framework

Year	Add-on course in Semiconductor Technology			Total Credits
	Core Courses	Dissertation/ Project work/ Apprenticeship /internship etc.	Value Added Course/ Employability &Entrepreneurship Skills Course	
I	CC- 1	PR- 1	SEC- 1	16

	4 Credits	4 Credits	4 Credits SEC- 2 4 Credits --	
II	CC- 2 4 Credits	PR- 2 4 Credits	SEC- 3 4 Credits SEC-4 4 Credits	16

YEAR-WISE BREAKUP

Year 1 – Add on Certificate Level course in Semiconductor Technology (16 Credits)

	Title	**Credits**
CC-1	Basic of Semiconductor and Electronics	4
SEC-1	Semiconductor Fabrication Course I	4
SEC-2	Semiconductor Fabrication Course II	4
PR-1	Laboratory Practical/Workshop/Internship/Project	4

Completion of Year 1 (16 Credits) → Add-on certificate **level** course in Semiconductor technology.

Year 2 – Add on Diploma Level course in Semiconductor Technology (Additional 16 Credits)

	Title	**Credits**
CC-2	Basics of VLSI and Microprocessor	4
SEC-3	Semiconductor Testing & Packaging I	4
SEC-4	Semiconductor Testing & Packaging II	4
PR-2	Laboratory Practical/Workshop/Internship/Project	4

Completion of Year 2 (Total 32 Credits) → Add-on Diploma **level** course in Semiconductor Technology.

8. Teaching-Learning Methods

Hybrid (Online/offline/MOOCs/online platforms) which includes combination of Lectures, Practicals, Seminars, Workshops and Projects

9. Assessment and Evaluation

Continuous Internal Evaluation: 30%

External Evaluation (similar to end term examination but examination on Demand):70%

Passing Criteria: Minimum 40% in each paper.

10. Attendance Requirement

Minimum 75% attendance is mandatory in each course component. However, if due to some unavoidable circumstances the attendance of the student falls short by 20% then same may be relaxed with the approval of the Vice-chancellor.

11. Grading System

Marks (%)	Grade Point	Grade	Classification
90-100	10	O	Outstanding
80-89	9	A^+	Excellent
70-79	8	A	Very Good
60-69	7	B^+	Good
50-59	6	B	Above Average
40-49	5	C	Average
<40	0	F	Fail

12. Award of Add-on Diploma **level course in Semiconductor Technology**

The Add-on Diploma **level course** in Semiconductor Technology be awarded to candidates who successfully earn the prescribed credits and meet the academic and attendance requirements.

13. OUTCOME OF THE COURSE

Add on Certificate Level Course Holders: Ready for entry-level roles in labs, semiconductor testing, and QA/QC.

Add-on Diploma Level Course Holders: Eligible for roles in semiconductor R&D, device fabrication units, startups, or can pursue higher research (PhD/MTech in VLSI/ Nanoelectronics).

14. Re-Appear/Improvement Policy: As per the Examination Rules of the University.

15. General Provisions

The University reserves the right to revise, modify or update the curriculum, rules, and structure from time to time.

Any issue not covered under this ordinance shall be decided by the Academic Council.

1st year

Course Type	Course Code	Nomenclature of course	Contact hours per week L: Lecture P: Practical			Internal Assessment Marks	End Term Examination Marks	Total Marks	Examination hours
			L	P	Total				
CC-1	25PHY-ST-101	Basic of Semiconductor Devices	4	0	4	30	70	100	3
SEC-1	25PHY-ST-102	Semiconductor Fabrication Course I	2	2	4	30	70	100	3
SEC-2	25PHY-ST-103	Semiconductor Fabrication Course II	2	2	4	30	70	100	3
PR-1	25PHY-ST-104	Laboratory Practical/Workshop/Internship/Project	0	4	4	30	70	100	3

2nd year

Course Type	Course Code	Nomenclature of course	Contact hours per week L: Lecture P: Practical			Internal Assessment Marks	End Term Examination Marks	Total Marks	Examination hours
			L	P	Total				
CC-2	25PHY-ST-201	Basics of VLSI and Microprocessor	3	1	4	30	70	100	3
SEC-3	25PHY-ST-202	Semiconductor Testing & Packaging I	3	1	4	30	70	100	3
SEC-4	25PHY-ST-203	Semiconductor Testing & Packaging II	3	1	4	30	70	100	3
PR-2	25PHY-ST-204	Laboratory Practical/Workshop/Internship/Project	0	4	4	30	70	100	3

Note: The Course type PR-1 and PR-2 represents the Laboratory Practical/Workshop/Internship/ Project, hence same will be decided based on the choice of the student and availability of the resources.

25PHY-ST-101
Basics of Semiconductor Devices

Maximum Marks-100
External Examination-70
Internal Assessment-30
Max. Time- 3 hrs.

Course Learning Outcomes
After completing this course, the learner will be able to:

1. **Understand the basic properties of semiconductor materials and explain the role of crystal structure in semiconductor behavior.**
2. **Analyze the energy band theory, including valence and conduction bands and calculate carrier concentration, mobility, conductivity, and Fermi level, and evaluate how these parameters vary with temperature and doping levels.**
3. **Illustrate the construction and working principles of PN junction diodes, and analyze their I-V characteristics and temperature dependence.**
4. **Compare and contrast different semiconductor devices such as diodes, LEDs, photodiodes, Zener diodes, and solar cells in terms of structure and operation.**
5. **Demonstrate understanding of bipolar junction transistors (BJTs), including NPN and PNP types, their characteristics, and applications.**
6. **Analyze the structure, working, and current-voltage characteristics of field-effect transistors (JFETs and MOSFETs), including pinch-off, gate control, and saturation.**

Note: *There shall be nine questions in all. Question no. 1 shall be compulsory, consisting of eight short answer type questions covering the entire syllabus out of which a candidate has to attempt any seven questions. A candidate has to attempt total five question in all. All questions carry equal marks.*

Introduction to Semiconductor material (Silicon, Germanium, Compound Semiconductors), conductors and insulators, crystal structures and their role in semiconductor materials, Energy band theory and the concept of valence and conduction bands, Doping: concept of doping and how it changes the properties of semiconductors,

PN Junction diode and their construction, Diode I-V characteristics, effect of temperature on semiconductors, Studying the process of creating ntype and p-type semiconductors, Intrinsic and Extrinsic Semiconductors, Concepts of electron and hole carriers in semiconductors, Calculating carrier concentration and mobility, Fermi level and its importance in carrier behaviour, doping affects on Fermi level, Conductivity in semiconductors and its temperature dependence, Carrier Generation and Recombination with impact on electrical behaviour of semiconductors, Thermal, mechanical, and electrical properties of semiconductor materials,

Semiconductor devices like diodes, transistors, and their principle of operation, Light Emitting Diode, Photodiode, Zener Diode; Solar cells, Bipolar Junction Transistors, NPN and PNP BJTs

and their characteristics, Hall Effect in Semiconductor material, Structures of n- and p-channel JFET, Pinch-off and saturation, Gate Control, Current Voltage characteristics, Structure and working principle of enhancement type and depletion type MOSFETs. Study the Seeback&Peltier Effect.

Suggested Books:

1. Sze, S.M. and Kwok, K. Ng, "Semiconductor Devices: Physics and Technology", Third Edition, John Wiley and Sons. 2007
2. Streetman, B.G., Banerjee, S. K. "Solid State Electronic Devices", Sixth Edition, PHI Learning Private Limited. 2013
3. Tyagi, M.S., "Semiconductor Materials and Devices", John Wiley and Sons. 2008
4. Millman J, Halkias C. C., Satyabrata J, "Electronic Devices & Circuits", Tata McGraw Hill 2007
5. Single Charge Tunneling: Coulomb Blockade Phenomena In Nanostructures by Hermann Grabert, Michel H. Devoret: Springer 1992

25-PHY-ST-102
Semiconductor Fabrication Technology I

Maximum Marks-100
External Examination-70
Internal Assessment-30
Max. Time- 3 hrs.

Course Learning Outcomes
After completing this course, the learner will be able to:

1. **Understand semiconductor materials and crystal growth.**
2. **Describe fabrication processes used in IC manufacturing.**
3. **Analyze lithography and etching techniques for nanoscale devices.**
4. **Apply knowledge of process integration and yield considerations.**
5. **Appreciate scaling limits, advanced nodes, and future fabrication technologies.**

Note: ***There shall be nine questions in all. Question no. 1 shall be compulsory, consisting of eight short answer type questions covering the entire syllabus out of which a candidate has to attempt any seven questions. A candidate has to attempt total five question in all. All questions carry equal marks.***

Introduction to cleanrooms; Semiconductor materials (silicon, gallium arsenide, gallium nitride, silicon carbide, etc) and their properties; Crystal lattices, bonding, and energy band structures; Cleanroom protocols, Safety procedures, and Environmental control

Introduction to doping; Basic concepts: Intrinsic vs. extrinsic semiconductors; Importance of impurity control; Ion implantation: Principles and process; Ion source and Ion generation; Ion acceleration; Mass spectrometry and Energy selection; Implant acivation and Rapid anneal; Precise control; Enabling technologies; Low-temperature process; Operational considerations and challenges; Doping profiles; Crystal damage; and Channeling; Masking issues.

Fundamentals of lithography, resists, and masks; Process steps: resist coating, Exposure, developing and baking; Minimum feature size and technology scaling; Projection lithography; Contact lithography; Resolution enhancement techniques; and Advanced techniques like electron-beam lithography (EBL).

Bulk Crystal Growth and Wafer Manufacturing; Thermal Oxidation; Rapid Thermal Processing (RTP); Furnaces; Deal-Grove Model for Thermal Oxidation; Semiconductor Dielectric Interface; Thermal Budget of Semiconductor Process.

LABORATORY / PRACTICAL COMPONENTS

The laboratory sessions for this course are designed to complement the theoretical concepts covered in lectures by providing hands-on experience with key semiconductor fabrication and

characterization techniques. The specific experiments to be conducted will be determined by the course instructor. However, the practical work will broadly cover the following areas:

- Wafer Cleaning:
- Oxidation and Thickness Measurement (Ellipsometry):
- Photolithography Pattern Transfer (Demonstration):
- Simulation:Use of semiconductor device simulation tools to model physical behavior and performance of basic semiconductor devices.

Suggested Books:

1. S. M. Sze (Ed.), *VLSI Technology* (2nd ed.). McGrawHill.
2. .Peter Van Zant, *Microchip Fabrication: A Practical Guide to Semiconductor Processing* (6th ed.). McGrawHill, 2014.
3. Stanley Wolf & Richard N. Tauber, *Silicon Processing for the VLSI Era* (Vols. 1–4). Lattice Press. .
4. Richard C. Jaeger, *Introduction to Microelectronic Fabrication.* (Modular Series on Solid State Devices).
5. James D. Plummer, Michael D. Deal & Peter B. Griffin, *Silicon VLSI Technology: Fundamentals, Practice, and Modeling.* Prentice Hall, 2000.

25-PHY-ST-103
Semiconductor Fabrication Technology II

Maximum Marks-100
External Examination-70
Internal Assessment-30
Max. Time- 3 hrs.

Course Learning Outcomes
After completing this course, the learner will be able to:

1. **Understand semiconductor materials and crystal growth.**
2. **Describe fabrication processes used in IC manufacturing.**
3. **Analyze lithography and etching techniques for nanoscale devices.**
4. **Apply knowledge of process integration and yield considerations.**
5. **Appreciate scaling limits, advanced nodes, and future fabrication technologies.**

Note: *There shall be nine questions in all. Question no. 1 shall be compulsory, consisting of eight short answer type questions covering the entire syllabus out of which a candidate has to attempt any seven questions. A candidate has to attempt total five question in all. All questions carry equal marks.*

Basics of deposition; Physical vapor deposition (PVD) methods (Sputtering, evaporation); Chemical vapor deposition (CVD) and atomic layer deposition (ALD); and Epitaxial growth.

Etching - Definition and purpose; Wet etching (Liquid chemicals); Dry etching (Plasma); Reactive ion etching (RIE) – Classification, mechanism, process, advantages and applications; CMP

Wafer preparation (e.g., metrology, contamination control); Photolithography & etching (e.g., pattern fidelity, etch uniformity); Deposition processes (e.g., film thickness, uniformity, defect inspection); Doping (e.g., implant dose, uniformity); Statistical process control (SPC) and Advanced quality control concept.

Foundational concepts of wafer yield; Defining wafer yield; Basics of wafer and die; The concept of defects; Yield modeling and calculation; Factors affecting wafer yield; Yield improvement and management; and Case studies and future trends.

Resistivity; Sheet resistance; Capictance; Conduction mechanisms; Electric Field Effect; Basic characterstics of diode and transistor; Breakdown voltage; Tunneling; Dielectric degradation; and Reliability.

LABORATORY / PRACTICAL COMPONENTS

The laboratory sessions for this course are designed to complement the theoretical concepts covered in lectures by providing hands-on experience with key semiconductor fabrication and

characterization techniques. The specific experiments to be conducted will be determined by the course instructor. However, the practical work will broadly cover the following areas:

- Deposition & Etching Techniques:
- Basics of wafer preparation
- Basics of semiconductor devices and performance monitoring

Suggested Books:

1. S. M. Sze (Ed.), *VLSI Technology* (2nd ed.). McGrawHill.
2. .Peter Van Zant, *Microchip Fabrication: A Practical Guide to Semiconductor Processing* (6th ed.). McGrawHill, 2014.
3. Stanley Wolf & Richard N. Tauber, *Silicon Processing for the VLSI Era* (Vols. 1–4). Lattice Press. .
4. Richard C. Jaeger, *Introduction to Microelectronic Fabrication*. (Modular Series on Solid State Devices).
5. James D. Plummer, Michael D. Deal & Peter B. Griffin, *Silicon VLSI Technology: Fundamentals, Practice, and Modeling*. Prentice Hall, 2000.

25-PHY-ST-201
Basic of VLSI and Microprocessor

Maximum Marks-100
External Examination-70
Internal Assessment-30
Max. Time- 3 hrs.

Course Learning Outcomes
After completing this course, the learner will be able to:

1. Provide an overview of the digital IC design techniques.
2. Understand the Difference between microprocessors and microcontrollers.
3. Understand the different microprocessors (8085 & 8086) with architecture and pin diagram.
4. Understand the working and programming of different (8085 & 8086) microprocessors

Note: ***There shall be nine questions in all. Question no. 1 shall be compulsory, consisting of eight short answer type questions covering the entire syllabus out of which a candidate has to attempt any seven questions. A candidate has to attempt total five question in all. All questions carry equal marks.***

Overview of VLSI Design: Historical perspective, overview of VLSI design methodologies, VLSI design flow, design hierarchy, concepts of regularity, modularity, and locality, VLSI design styles, design quality, packaging technology, CAD technology. MOS Transistor Theory: Introduction to The metal oxide semiconductor (MOS) structure, Long-channel I-V characteristics, C-V characteristics, non-linear I-V effects, DC transfer characteristics.

Difference between microprocessors and microcontrollers, Types of Micro-controllers,Evolution of microprocessors, Microprocessor internal architecture, hardware model of 8085, Pin diagram, Instruction set, Programming model of 8085, Addressing modes, Assembly language programming, Timing Diagram, Peripheral I/O, Memory mapped I/O, 8085 Interrupts, Stack and subroutines.

Architecture, Pin diagram, Physical address, Segmentation, Memory organization, addressing modes, Instruction set, Assembly language programming of 8086, Comparison of 8086 & 8088 microprocessor.

LABORATORY / PRACTICAL COMPONENTS

The laboratory sessions for this course are designed to complement the theoretical concepts covered in lectures by providing hands-on experience with key semiconductor fabrication and characterization techniques. The specific experiments to be conducted will be determined by the course instructor. However, the practical work will broadly cover the use if ICs in various circuits and microprocessor like 8085, 8086 etc.:

Suggested Books:

1. N. H. E. Weste and C. Harris, "Principles of CMOS VLSI Design: A System Perspective, 3rd Edition, Pearson Education 2007.
2. Ramesh Gaonkar, "Microprocessor Architecture, Programming, and Applications with the 8085", Penram International Publication (India) Pvt. Ltd.
3. A. K. Ray & K. M. Bhurchandi, "Advanced Microprocessors andperipherals", Tata McGraw Hill.
4. Barry B. Brey, "The Intel Microprocessors Architecture Programming and interfacing", Pearson.

25-PHY-ST-202
Semiconductor Packaging and Testing I

Maximum Marks-100
External Examination-70
Internal Assessment-30
Max. Time- 3 hrs.

Course Learning Outcomes
After completing this course, the learner will be able to:

1. Explain the role and importance of packaging in semiconductor devices.
2. Analyze packaging materials and their properties.
3. Describe packaging techniques, assembly, and interconnect technologies.
4. Evaluate reliability, testing, and thermal management approaches.
5. Understand current challenges and opportunities in advanced packaging.

Note: ***There shall be nine questions in all. Question no. 1 shall be compulsory, consisting of eight short answer type questions covering the entire syllabus out of which a candidate has to attempt any seven questions. A candidate has to attempt total five question in all. All questions carry equal marks.***

Role of packaging in microelectronics; Functions of packaging (mechanical support, electrical connections, thermal dissipation, environmental protection); Historical evolution: DIP, QFP, BGA, CSP to Fan-out WLP, 2.5D/3D IC; Industry ecosystem (IDMs, OSATs, Foundries)

Substrate materials: ceramics, organics, laminates, silicon interposers; Encapsulation materials: molding compounds, underfills, adhesives; Conductive materials: solders, lead-free alloys, conductive adhesives; Die attach, wire-bonding wires (Au, Cu, Al), redistribution layers; Material properties: CTE, modulus, thermal conductivity, reliability concerns

Conventional packaging: Wire bonding, Leaded packages (DIP, SOIC, QFP), Ball Grid Arrays (BGA, FBGA, LGA); Advanced packaging: Flip-chip bonding, Wafer Level Packaging (WLP, Fan-In/Fan-Out), System-in-Package (SiP), 2.5D/3D IC integration, TSV (Through-Silicon Vias); MEMS and sensor packaging

Electrical design considerations (signal integrity, power integrity, parasitics); Thermal management (heat dissipation, thermal modeling, TIMs, heat sinks); Mechanical stress and warpage control; Reliability aspects in high-density packaging

Package-level reliability testing (temperature cycling, HAST, drop/shock tests); Failure analysis techniques (X-ray, SAM, FIB, cross-sectioning); Burn-in, test sockets, probe technologies; Standards: JEDEC, IPC, MIL-STD, RoHS, REACH

LABORATORY / PRACTICAL COMPONENTS

The laboratory sessions for this course are designed to complement the theoretical concepts covered in lectures by providing hands-on experience with key semiconductor fabrication and characterization techniques. The specific experiments to be conducted will be determined by the course instructor. However, the practical work will broadly cover the following areas:

- Wire bonding and die attach
- Flip-chip assembly simulation
- Thermal analysis using ANSYS/Icepak
- Failure analysis case studies
- Package modeling using COMSOL / HFSS

Suggested Books:

1. Rao R. Tummala, *Fundamentals of Microsystems Packaging*. McGrawHill, 1st ed., 2001.
2. John H. Lau (et al.), *Advanced MEMS Packaging*, 1st ed. McGrawHill, 2010.
3. John H. Lau, *Semiconductor Advanced Packaging*, Springer, 2021. ISBN 9789811613753
4. Ephraim Suhir, *Microelectronics Packaging: Emission, Reliability, and Design*
5. Charles A. Harper, *Electronic Packaging and Interconnection Handbook*, 4th edition. McGrawHill, 2005.
6. **Standards:** JEDEC/ IPC standards and handbooks

25-PHY-ST-203
Semiconductor Packaging and Testing II

Maximum Marks-100
External Examination-70
Internal Assessment-30
Max. Time- 3 hrs.

Course Learning Outcomes
After completing this course, the learner will be able to:

1. **Understand the semiconductor manufacturing and testing lifecycle.**
2. **Explain the types and levels of testing for semiconductor devices.**
3. **Use ATE (Automatic Test Equipment) principles and tools.**
4. **Perform basic fault diagnosis and yield analysis.**
5. **Evaluate test economics and design-for-testability (DFT).**
6. **Understand current challenges and opportunities in advanced packaging.**

Note: *There shall be nine questions in all. Question no. 1 shall be compulsory, consisting of eight short answer type questions covering the entire syllabus out of which a candidate has to attempt any seven questions. A candidate has to attempt total five question in all. All questions carry equal marks.*

Heterogeneous integration, chiplets, RDL-based fan-out; AI, 5G, automotive electronics packaging requirements; Advanced interconnects (copper pillars, hybrid bonding, optical interconnects); Sustainability and green packaging materials; Case studies from Intel, TSMC, Amkor, ASE

What is semiconductor testing; Why testing is critical (cost, quality, reliability); Overview of IC manufacturing and test flow; Wafer vs. package vs. system-level testing; Wafer Test (Probe Test); Package Test (Final Test); Burn-In Testing; System-Level Testing (SLT) and Environmental and Reliability Testing (HTOL, HAST, ESD, Latch-Up)

What is ATE; Structure of ATE systems (DUT board, handler, prober); Key players: Advantest, Teradyne, NI, etc.; Test interfaces (JTAG, SPI, I2C); Role of testers in production; What is DFT; Scan chains and scan insertion; Boundary Scan (JTAG/IEEE 1149.1); Built-In Self-Test (BIST); Memory BIST (MBIST), Logic BIST (LBIST)

Digital testing: scan chain, BIST, pattern generation; Analog/Mixed-signal testing: parametric testing, loopback and Challenges of analog test (accuracy, repeatability)

Yield metrics: gross yield, test yield, final yield; Test time vs. cost tradeoffs; Test escape and DPPM (Defective Parts Per Million); Root cause analysis; Reliability screening (burn-in, temp cycling); EDA tools for DFT (Synopsys, Cadence, Siemens EDA); AI/ML

in semiconductor testing; Post-silicon debug and silicon bring-up and Careers in semiconductor test

LABORATORY / PRACTICAL COMPONENTS

The laboratory sessions for this course are designed to complement the theoretical concepts covered in lectures by providing hands-on experience with key semiconductor fabrication and characterization techniques. The specific experiments to be conducted will be determined by the course instructor. However, the practical work will broadly cover the following areas:

- Test and burn-in socket demo
- Simple chip testing demo
- Test modeling

Suggested Books:

1. Latest JEDEC/IPC Standards
2. IEEE papers on VLSI testing
3. Access to open-source test simulation tools
4. Sample test vector files and ATE logs